# PCI-1713

32-channel Isolated
Analog Input Card

*User's manual*

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**CE notification**
The PCI-1713, developed by ADVANTECH CO., LTD., has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

**On-line Technical Support**
For technical support and service please visit out support website at **http://support.advantech.com**

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CHAPTER 1

# General Information

# 1.1 Introduction

The PCI-1713 is a 12-bit 32-channel analog input card for the PCI bus. It provides 32 analog input channels with a sampling rate up to 100k samples/s, 12-bit resolution and isolation protection of 2500 $V_{DC}$.

## PCI-bus Plug and Play

The PCI-1713 uses a PCI controller to interface the card with the PCI bus. The controller fully implements the PCI bus specification Rev 2.1. All bus relative configurations, such as base address and interrupt assignment, are automatically controlled by software.

## Flexible Input Types and Range Settings

The PCI-1713 features an automatic channel/gain scanning circuit. The circuit, rather than your software, controls multiplexer switching during sampling. The on-board SRAM stores different gain values and configurations for each channel. This design lets you perform multi-channel sampling with different gains for each channel and with free combination of single-ended and differential inputs.

## High-speed Data Acquisition

The PCI-1713 provides a sampling rate up to 100k samples/s. It has an on-board FIFO buffer, which can store up to 4K A/D samples and generates an interrupt signal when the FIFO is half full. This feature provides continuous high-speed data transfer and more predictable performance on Windows systems.

## Supports S/W, Internal and External Pacer Triggering

The PCI-1713 supports three kinds of trigger modes for A/D conversion: software triggering, internal pacer triggering and external pacer triggering. The software trigger allows users to acquire a sample when it is needed; the internal pacer triggers continuous high-speed data acquisition. The PCI-1713 also accepts external trigger sources, allowing synchronous sampling with external devices.

### Satisfies the Need for Isolation Protection

The PCI-1713 provides optical isolation protection of 2500 $V_{DC}$ between the inputs and the PC bus to protect the PC and peripherals from damage due to high voltages on the input lines. It is ideal for the situations where budget-conscious users require flexibility, stability and a high level of isolation protection for their data acquisition system.

## 1.2 Features

- 32 single-ended or 16 differential analog inputs, or a combination
- 12-bit A/D converter, with up to 100 kHz sampling rate
- Programmable gain for each input channel
- Automatic channel/gain scanning
- On-board 4K samples FIFO buffer
- Programmable pacer

## 1.3 Specifications

### Analog Input:

- **Channels:** 32 single-ended or 16 differential (software programmable)
- **Resolution:** 12-bit
- **On-board FIFO:** 4K samples
- **Conversion time:** 2.5 μs
- **Input range:**

  Bipolar: ±10 V, ±5 V, ±2.5 V, ±1.25 V, ±0.625 V

  Unipolar: 0 ~10 V, 0 ~ 5 V, 0 ~ 2.5 V, 0 ~ 1.25 V

- **Maximum Input Overvoltage:** ±30 V
- **Common Mode Rejection Ratio (CMRR)**

| Gain | CMRR |
|---|---|
| 0.5, 1 | 75dB |
| 2 | 80dB |
| 4 | 84dB |
| 8 | 84dB |

- **Maximum sampling rate:** 100 kHz
- **Accuracy:** (depending on gain)

| Gain | Accuracy |
|---|---|
| 0.5, 1 | 0.01% of FSR±1LSB |
| 2 | 0.02% of FSR±1LSB |
| 4 | 0.02% of FSR±1LSB |
| 8 | 0.04% of FSR±1LSB |

- **Linearity error:** ±1 LSB
- **Drift:** Typical 30 PPM / °C ( 0 ~ 60 °C )
- **Input impedance:** 1 GΩ
- **Trigger mode:** Software, on-board programmable pacer or external
- **Trigger Input:** TTL level

## Programmable Timer/Counter

- **Counter chip:** 82C54 or equivalent
- **Counters:** 3 channels, 16 bits
  2 channels are permanently configured as programmable pacers;
  1 channel is un-used.
- **Time base:**

  Channel 1:10 MHz

  Channel 2:Takes input from output of channel 1

  Channel 0:un-used.

## General:

- **I/O Connector:** 37-pin D-type female connector
- **Dimensions:** 175 mm x 100 mm (6.9" x 3.9")
- **Power consumption:** +5 V @ 850 mA (Typical),
  +5 V @ 1.0 A (Max.)
- **Operating temperature:** 0 ~ +60 °C (32 ~ 140 °F) ( refer to IEC 68-2-1, 2 )
- **Storage temperature:** -20 ~ +70 °C (-4 ~ 158 °F)
- **Operating humidity:** 5 ~ 95%RH non-condensing ( refer to IEC 68-2-3 )
- **MTBF:** over 85,310 hrs @ 25 °C, grounded, fixed environment

# 1.4 Block Diagram

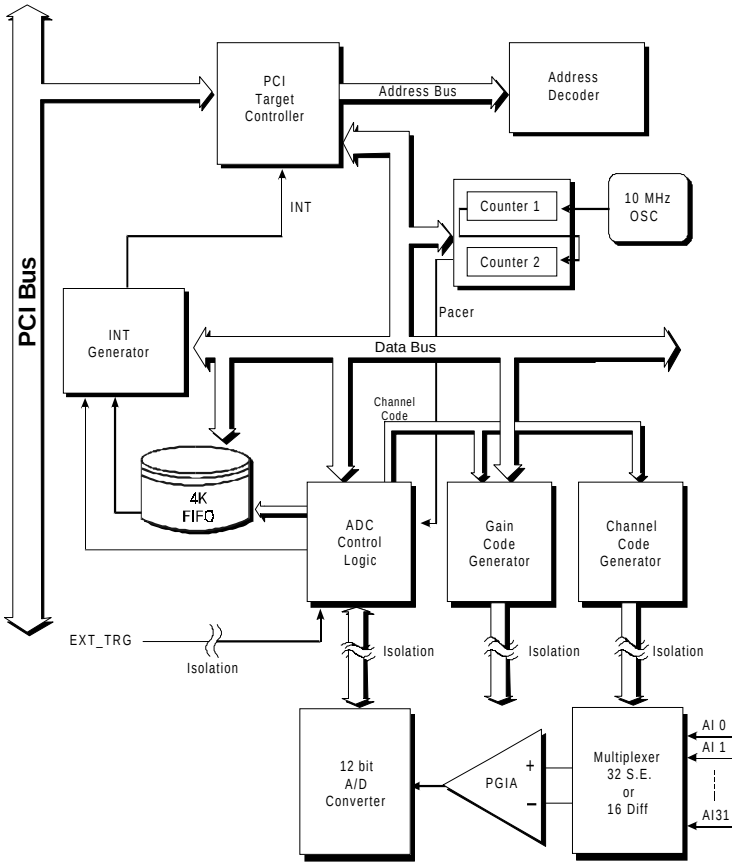



**Figure 1-1: PCI-1713 block diagram**

CHAPTER 2

# Installation

## 2.1 Initial Inspection

Before installing the PCI-1713, check the card for visible damage. We have carefully inspected the card both mechanically and electrically before shipment. It should be free of marks and in perfect order upon receipt.

As you unpack the PCI-1713, check it for signs of shipping damage (damaged box, scratches, dents, etc.). If it is damaged or fails to meet specifications, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing materials for inspection by the carrier. We will then make arrangements to repair or replace the unit.

## 2.2 Unpacking

The PCI-1713 contains components that are sensitive and vulnerable to static electricity. Discharge any static electricity on your body to ground by touching the back of the system unit (grounded metal) before you touch the board.

Remove the PCI-1713 card from its protective packaging by grasping the card's rear panel. Handle the card only by its edges to avoid static discharge which could damage its integrated circuits. Keep the antistatic package. Whenever you remove the card from the PC, protect the card by storing it in this package.

You should also avoid contact with materials that hold static electricity such as plastic, vinyl and styrofoam.

Check the product contents inside the packing. There should be one card, one CD-ROM, and this manual. Make sure nothing is missing.

## 2.3 Installation Instructions

The PCI-1713 can be installed in any PCI slot in the computer. However, refer to the computer user's manual to avoid any mistakes and danger before you follow the installation procedure below:

1. Turn off your computer and any accessories connected to the computer.

***Warning!*** *TURN OFF your computer power supply whenever you install or remove any card, or connect and disconnect cables.*

2. Disconnect the power cord and any other cables from the back of the computer.
3. Remove the cover of the computer.
4. Select an empty +5 V PCI slot. Remove the screw that secures the expansion slot cover to the system unit. Save the screw to secure the interface card retaining bracket.
5. Carefully grasp the upper edge of the PCI-1713. Align the hole in the retaining bracket with the hole on the expansion slot and align the gold striped edge connector with the expansion slot socket. Press the card into the socket gently but firmly. Make sure the card fits the slot tightly.
6. Secure the PCI-1713 by screwing the mounting bracket to the back panel of the computer.
7. Attach any accessories (37-pin D-type cable, wiring terminal board, etc.) to the card.
8. Replace the cover of your computer. Connect the cables you removed in step 2.
9. Turn the computer power on.

CHAPTER 3

# Signal Connections

# 3.1 Overview

Correct signal connections are one of the most important factors in ensuring that your application system is sending and receiving data correctly. A good signal connection can avoid much unnecessary and costly damage to your valuable PC and other hardware devices. This chapter will provide some useful information about how to connect analog input signals to the PCI-1713 card via the I/O connector.

# 3.2 I/O Connector

The I/O connector for the PCI-1713 card is a 37-pin D-type connector which you can connect to 37-pin D-type accessories with Advantech's PCL-10137 cable.

***Note!:*** *The PCI-1713 does not include the PCL-10137 cable assembly.*

The following figure shows the pin assignments for the 37-pin I/O connector on the PCI-1713 card.

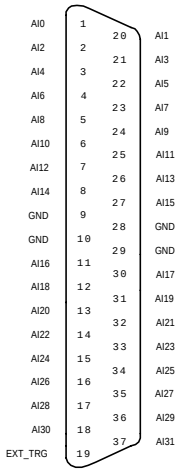



**Figure 3-1: I/O connector pin assignments for the PCI-1713 card**

## I/O Connector Signal Descriptions

| Signal Name | Reference | Direction | Description |
|---|---|---|---|
| AI<0…31> | GND | Input | **Analog Input Channels 0 through 31.** Each channel pair, AI<i, i+1> (i = 0, 2, 4...30), can be configured as either two single-ended inputs or one differential input. |
| GND | - | - | **Ground**. These pins are the reference points for single-ended measurements and the bias current return point for differential measurement. |
| EXT_TRG | GND | Input | **A/D External Trigger.** This pin is the external trigger signal input for the A/D conversion. A low-to-high edge triggers A/D conversion to happen. |

# 3.3 Analog Input Connections

This section continues to describe how to make analog input signal connections to the PCI-1713 card via the I/O connector.

## Single-ended Channel Connections

The single-ended input configuration has only one signal wire for each channel, and the measured voltage (Vm) is the voltage of the wire referred to the common ground.
A signal source without a local ground is also called a “floating source”. It is fairly simple to connect a single-ended channel to a floating signal source. In this mode, the PCI-1713 card provides a reference ground for external floating signal sources.

Figure 3-2 shows a single-ended channel connection between a floating signal source and an input channel on the PCI-1713 card.

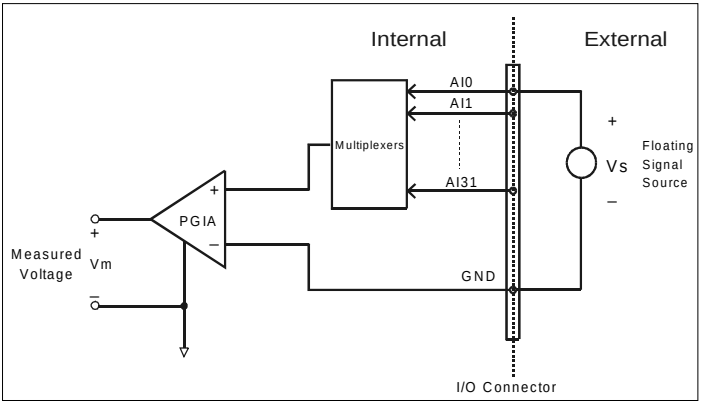



**Figure 3-2: Single-ended input channel connection**

## Differential Channel Connections

The differential input configuration has two signal wires for each channel, and the differential input responds only to voltage differences between High and Low inputs. On the PCI-1713 card, when all channels are configured to differential input, up to 16 analog channels are available.

If one side of the signal source is connected to a local ground, the signal source is ground-referenced. The ground of the signal source and the ground of the PCI-1713 will not be at exactly the same voltage, as they are connected through the ground return of the equipment and building wiring. The difference between the ground voltages forms a common-mode voltage ($V_{cm}$).

To avoid the ground loop noise effect caused by common-mode voltages, you can connect the signal ground to the Low input. Figure 3-3 shows a differential channel connection between a ground-referenced signal source and an input channel on the PCI-1713 card. With this connection, the PGIA rejects a common-mode voltage $V_{cm}$ between the signal source and the PCI-1713 ground, shown as $V_{cm}$ in Figure 3-3.

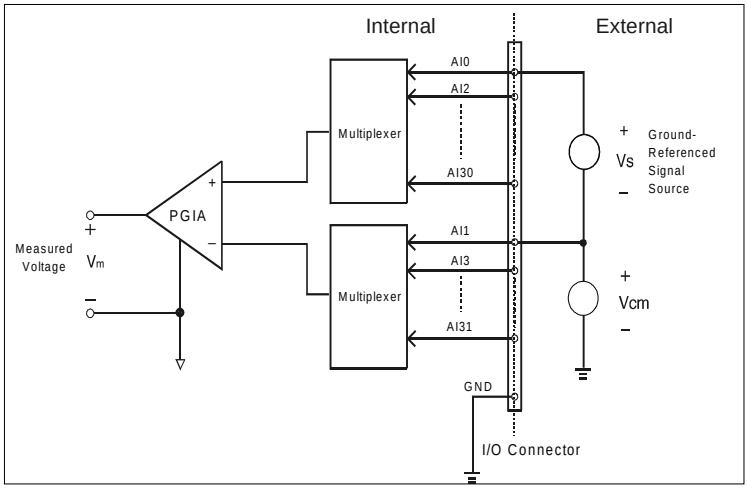



**Figure 3-3: Differential input channel connection with grounded referenced signal source**

If a floating signal source is connected to the differential input channel, the signal source may exceed the common-mode signal range of the PGIA, and the PGIA will be saturated with erroneous voltage-readings. You must therefore reference the signal source to the AIGND.

Figure 3-4 shows a differential channel connection between a floating signal source and an input channel on the PCI-1713 card. In this figure, each side of the floating signal source is connected through a resistor to the AIGND. This connection can reject the common-mode voltage between the signal source and the PCI-1713 card ground.

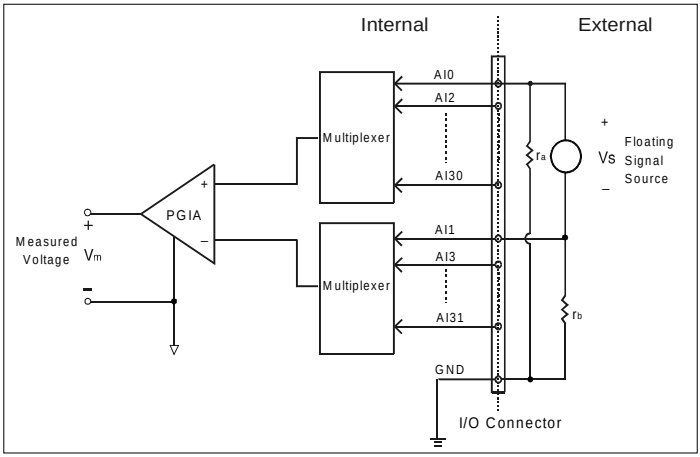
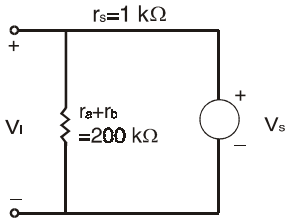



**Figure 3-4: Differential input channel connection- floating signal source**




$V_s$: ideal signal source

$V_I$: measured signal source

$r_s$: output impedance of signal source

$r_a$, $r_b$: series-wound resistors

$$V_I = \frac{r_a+r_b}{r_s+r_a+r_b} V_s = \frac{200}{1+200} V_s = \frac{200}{201} V_s$$

$$\text{Gain error} = \frac{V_i-V_s}{V_s} = -\frac{1}{201} = -0.5\%$$

### External Trigger Source Connection

In addition to pacer triggering, the PCI-1713 card also allows external triggering for A/D conversions. A low-to-high edge coming from EXT_TRG will trigger an A/D conversion on the PCI-1713 board.

***Note!:*** *Don't connect any signal to the EXT_TRG pin when the external trigger function is not being used.*

***Note!:*** *If you use external triggering for A/D conversions, we recommend you choose differential mode for all analog input signals, so as to reduce the cross-talk noise caused by the external trigger source.*

## 3.4 Field Wiring Considerations

When you use the PCI-1713 card to acquire outside data, environmental noise can seriously affect the accuracy of your measurements if you don't provide any protection. The following suggestions will be helpful when running signal wires between signal sources and the PCI-1713 card.

- Please make sure that you have carefully routed signal cables to the card. You must separate the cabling from noise sources. Try to keep video monitors far away from the analog signal cables, because these are a common noise source in a PCI data acquisition system.
- If you want to reduce common-mode noise, try to use differential analog input connections.
- If you do not want your signals to be affected when travelling through areas with high electromagnetic interference or large magnetic fields, try the following routing techniques: Use individually shielded, twisted-pair wires to connect analog input signals to the board, i.e. the signals connected to the High and Low inputs are twisted together and covered with a shield. Finally, connect the shield only to one point at the signal source ground.

- Make sure that your signal lines do not travel through conduits, because these may contain power lines. Also, keep your signals far from electric motors, breakers or welding equipment, as these can create magnetic fields.
- Keep a reasonable distance between high-voltage (or high-current) lines and signal cables connected to the PCI-1713 card if the cables run parallel, or route signal cables at right angles to high voltage/current cables.

CHAPTER 4

# Register Structure and Format

# 4.1 Overview

The PCI-1713 is delivered with an easy-to-use 32-bit DLL driver for user programming under the Windows 98/95/NT operating system. We advise users to program the PCI-1713 using the 32-bit DLL driver provided by Advantech to avoid the complexity of low-level programming by register.

The most important consideration in programming the PCI-1713 card at a register level is to understand the function of the card's registers. The information in the following sections is provided only for users who would like to do their own low-level programming.

# 4.2 I/O Port Address Map

The PCI-1713 card requires 18 addresses in the PC's I/O space. The address of each register is specified as an offset from the card's base address. For example, BASE+0 is the card's base address and BASE+7 is the base address plus seven bytes.

Table 4-1 shows the function of each register and its address relative to the card's base address.

**Table 4-1: PCI-1713 register format (Part 1)**

| Base Address + decimal | Read | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Channel Number and A/D Data | | | | | | | |
| 1 | | | | | AD11 | AD10 | AD9 | AD8 |
| 0 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| | N/A | | | | | | | |
| 3 | | | | | | | | |
| 2 | | | | | | | | |
| | N/A | | | | | | | |
| 5 | | | | | | | | |
| 4 | | | | | | | | |
| | Status Register | | | | | | | |
| 7 | | | | | IRQ | F/F | F/H | F/E |
| 6 | | | ONE/FH | IRQEN | GATE | EXT | PACER | SW |
| | N/A | | | | | | | |
| 9 | | | | | | | | |
| 8 | | | | | | | | |
| | Counter 0 | | | | | | | |
| 25 | | | | | | | | |
| 24 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | Counter 1 | | | | | | | |
| 27 | | | | | | | | |
| 26 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | Counter 2 | | | | | | | |
| 29 | | | | | | | | |
| 28 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | N/A | | | | | | | |
| 31 | | | | | | | | |
| 30 | | | | | | | | |

**Table 4-1: PCI-1713 register format (Part 2)**

| Base Address + decimal | Write | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | **Software A/D Trigger** | | | | | | | |
| 1 | | | | | | | | |
| 0 | | | | | | | | |
| | **A/D Channel Range Setting** | | | | | | | |
| 3 | | | | | | | | |
| 2 | | | S/D | B/U | | G2 | G1 | G0 |
| | **MUX Control** | | | | | | | |
| 5 | | | | Stop channel | | | | |
| 4 | | | | Start channel | | | | |
| | **Control Register** | | | | | | | |
| 7 | | | | | | | | |
| 6 | | | ONE/FH | IRQ | GATE | EXT | PACER | SW |
| | **Clear Interrupt and FIFO** | | | | | | | |
| 9 | clear FIFO | | | | | | | |
| 8 | clear interrupt | | | | | | | |
| | **Counter 0** | | | | | | | |
| 25 | | | | | | | | |
| 24 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | **Counter 1** | | | | | | | |
| 27 | | | | | | | | |
| 26 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | **Counter 2** | | | | | | | |
| 29 | | | | | | | | |
| 28 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | **Counter Control** | | | | | | | |
| 31 | | | | | | | | |
| 30 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

## 4.3 A/D Data — BASE + 0 and BASE + 1

These two bytes, BASE+0 and BASE+1, hold the result of A/D conversion data. The 12 bits of data from the A/D conversion are stored in BASE+1 bit 3 to bit 0 and BASE+0 bit 7 to bit 0.

**Table 4-2: Register for channel number and A/D data**

| Read | A/D Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BASE+1 | | | | | AD11 | AD10 | AD9 | AD8 |
| BASE+0 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |

**AD11 ~ AD0** Result of A/D Conversion

AD0 is the least significant bit (LSB) of the A/D data, and AD11 is the most significant bit (MSB).

## 4.4 Software A/D Trigger — BASE + 0

You can trigger an A/D conversion by software, the card's on-board pacer or an external pulse. Bit 2 to bit 0 of register BASE+6 can select the trigger source (see page 27 and page 28 for the register layout of BASE+6 and programming information). If you select software triggering, a write to the register BASE+0 with any value will trigger an A/D conversion.

## 4.5 A/D Channel Range Setting — BASE + 2

Each A/D channel has its own input range, controlled by a range code stored in the on-board RAM. If you want to change the range code for a given channel, select the channel as the start channel and the stop channel in the registers of BASE+4 and BASE+5 (described in the next section), and then write the range code to BASE+2 bit 0 to bit 2 and bit 4.

**Table 4-3: Register for A/D channel range setting**

| Write | A/D channel range setting | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BASE+2 | | | S/D | B/U | | G2 | G1 | G0 |

**S/D** Single-ended or Differential

0 means the channel is single-ended, and 1 means it is differential.

**B/U** Bipolar or Unipolar

0 means the channel is bipolar, and 1 means it is unipolar.

**G2 to G0** Gain Code

The following table lists the gain codes for the PCI-1713:

**Table 4-4: Gain codes for the PCI-1713**

| PCI-1713 | | | | | |
|---|---|---|---|---|---|
| Input Range(V) | Gain | B/U | Gain Code | | |
| | | | G2 | G1 | G0 |
| -5 to +5 | 1 | 0 | 0 | 0 | 0 |
| -2.5 to +2.5 | 2 | 0 | 0 | 0 | 1 |
| -1.25 to +1.25 | 4 | 0 | 0 | 1 | 0 |
| -0.625 to +0.625 | 8 | 0 | 0 | 1 | 1 |
| -10 to 10 | 0.5 | 0 | 1 | 0 | 0 |
| | N/A | 0 | 1 | 0 | 1 |
| | N/A | 0 | 1 | 1 | 0 |
| | N/A | 0 | 1 | 1 | 1 |
| 0 to 10 | 1 | 1 | 0 | 0 | 0 |
| 0 to 5 | 2 | 1 | 0 | 0 | 1 |
| 0 to 2.5 | 4 | 1 | 0 | 1 | 0 |
| 0 to 1.25 | 8 | 1 | 0 | 1 | 1 |
| | N/A | 1 | 1 | 0 | 0 |
| | N/A | 1 | 1 | 0 | 1 |
| | N/A | 1 | 1 | 1 | 0 |
| | N/A | 1 | 1 | 1 | 1 |

## 4.6 MUX Control—BASE + 4 and BASE + 5

**Table 4.5: The register for multiplexer control**

| Write | MUX Control | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BASE+5 | | | | CH4 | CH3 | CH2 | CH1 | CH0 |
| BASE+4 | | | | CL4 | CL3 | CL2 | CL1 | CL0 |

**CL4 ~ CL0** Start Scan Channel Number

**CH4 ~ CH0** Stop Scan Channel Number

BASE+4 bit 4 to bit 0, CL4 ~ CL0, act as a pointer when you program the A/D channel setting (see previous section). When you set the MUX start channel to an analog input channel, AIn ( n = 0, 1, 2, 3,..., 31), the gain code, B/U and S/D written to the register of BASE+2, is for channel n.

***Caution!*** *We recommend you set the same start and stop channel when writing to the register BASE+2. Otherwise, if the A/D trigger source is on, the multiplexer will continuously scan between channels and the range setting may be set to an unexpected channel. Make sure the A/D trigger source is turned off to avoid this kind of error.*

The write-only registers of BASE +4 and BASE+5 control how the multiplexers (MUXs) scan. BASE+4 bit 4 to bit 0, CL4 ~ CL0, hold the start scan channel number, and BASE+5 bit 4 to bit 0, CH4 ~ CH0, hold the stop scan channel number. Writing to these two registers automatically initializes the scan range of the MUXs. Each A/D conversion trigger also sets the MUXs to the next channel. With continuous triggering, the MUXs will scan from the start channel to the stop channel and then repeat. The following examples show the scan sequences of the MUXs (all channels are set as single-ended).

**Example 1** If the start scan input channel is AI3 and the stop scan input channel is AI7, then the scan sequence is AI3, AI4, AI5, AI6, AI7, AI3, AI4, AI5, AI6, AI7, AI3, AI4…

**Example 2** If the start scan channel is AI29 and the stop scan channel is AI2, then the scan sequence is AI29, AI30, AI31, AI0, AI1, AI2, AI29, AI30, AI31, AI0, AI1, AI2, AI29, AI30…

This scan logic of the PCI-1713 card is quite powerful and easily understood. You can respectively set the gain code, B/U and S/D, for each channel. The scan logic will be a little complex if you set the analog input channels in differential mode, however. In differential mode, signals are transmitted by a pair of channels, AI<i, i+1> ( i = 0, 2, 4,..., 30) . In each pair of differential channels, the even channel is the positive end and the odd one is the negative end.

For example, if channel 0 is set as differential, then channel 0 and channel 1 are combined into one channel and refer to the gain code and B/U of channel 0 (the channel 1 values are unavailable). By the same rule, if channel 2 is set as differential, then channel 2 and channel 3 are combined into one channel, and refer to the gain code and B/U of channel 2 (the channel 3 values are unavailable). The following examples show the scan sequences in differential mode.

**Example 3** Suppose that the start scan input channel is AI30 and the stop scan input channel is AI3. If AI30 is differential, AI0 and AI1 are single-ended, and AI2 is differential, then the scan sequence is AI30, AI0, AI1, AI2, AI30, AI0, AI1, AI2, AI30…..

**Example 4** Suppose that the start scan channel is AI27 and the stop scan channel is AI131. If AI27 is single-ended, AI28 is differential, and AI30 is differential, then the scan sequence is AI27, AI28, AI30, AI27, AI28, AI30, AI27…

***Warning!*** *Only even channels can be set as differential. An odd channel will become unavailable if its preceding channel is set as differential.*

# 4.7 Control Register — BASE + 6

The write-only register BASE+6 allows users to set an A/D trigger source and an interrupt source.

**Table 4-6: Control register**

| Write | Control Register | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BASE + 6 | | | ONE/FH | IRQEN | GATE | EXT | PACER | SW |

**SW** Software trigger enable bit

Set 1 to enable software trigger, and set 0 to disable.

**PACER** PACER trigger enable bit

Set 1 to enable pacer trigger, and set 0 to disable.

**EXT** External trigger enable bit

Set 1 to enable external trigger, and set 0 to disable.

***Note!:*** *Users cannot enable SW, PACER and EXT concurrently.*

**GATE** External trigger gate function enable bit

Set 1 to enable external trigger gate function, and set 0 to disable.

**IRQEN** Interrupt enable bit

Set 1 to enable interrupt, and set 0 to disable.

**ONE/FH** Interrupt source bit

Set 0 to interrupt when an A/D conversion occurs, and set 1 to interrupt when the FIFO is half full.

## 4.8 Status Register — BASE + 6 and BASE + 7

The registers of BASE+6 and BASE+7 provide information for the A/D configuration and operation.

**Table 4-7: Status register**

| Read | Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BASE+7 | | | | | IRQ | F/F | F/H | F/E |
| BASE+6 | | | ONE/FH | IRQEN | GATE | EXT | PACER | SW |

The content of the status register of BASE+6 is the same as that of the control register.

**F/E** FIFO Empty flag

This bit indicates whether the FIFO is empty. 1 means that the FIFO is empty.

**F/H** FIFO Half-full flag

This bit indicates whether the FIFO is half-full. 1 means that the FIFO is half-full.

**F/F** FIFO Full flag

This bit indicates whether the FIFO is full. 1 means that the FIFO is full.

**IRQ** Interrupt flag

This bit indicates the interrupt status. 1 means that an interrupt has occurred.

## 4.9 Clear Interrupt and FIFO — BASE + 8 and BASE + 9

Writing data to either of these two bytes clears the interrupt or the FIFO.

**Table 4-8: Registers to clear interrupt and FIFO**

| Write | Clear Interrupt and FIFO | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BASE+9 | Clear FIFO | | | | | | | |
| BASE+8 | Clear Interrupt | | | | | | | |

## 4.10 Programmable Timer/Counter Registers — BASE + 24, BASE + 26, BASE + 28 and BASE + 30

The four registers of BASE+24, BASE+26, BASE+28 and BASE+30 are used for the 82C54 programmable timer/counter. Please refer to Appendix A data sheets for detailed application information.

***Note!:*** *Users have to use a 16-bit (word) command to read/write each register.*

CHAPTER 5

# Calibration

# 5.1 Introduction

Regular calibration checks are important to maintain accuracy in data acquisition and control applications. To assist users in the A/D calibration process, we provide one calibration program, ADCAL.EXE, on the PCI-1713 software CD-ROM.

The ADCAL.EXE program makes A/D calibrations easy. It leads you through the calibration and setup procedure with a variety of prompts and graphic displays, showing you all of the correct settings and adjustments. This chapter offers a brief guide to these calibration programs.

To perform a satisfactory calibration, you need a $4^1/_2$-digit digital multimeter and a voltage calibrator or a stable, noise free D. C. voltage source.

# 5.2 VR Assignment

There are four variable resistors (VRs) on the PCL-1713 card. They help you to make accurate adjustments on all A/D channels. Please refer to the following figure for VR positions.

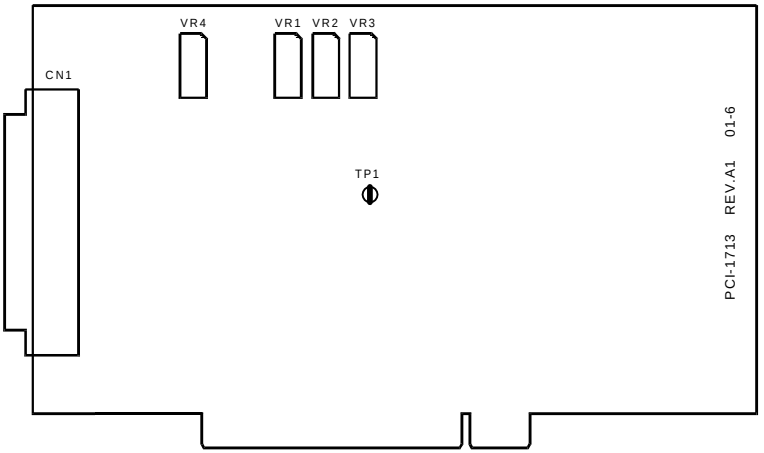


**Figure 5-1: PCL-1713 VR assignment**

The following list shows the function of each VR:

| VR | Function |
|---|---|
| VR1 | A/D full scale (gain) |
| VR2 | A/D bipolar offset |
| VR3 | A/D unipolar offset |
| VR4 | PGIA initial offset |
| TP1 | PGIA output |

## 5.3 A/D Calibration

Regular and accurate calibration procedures ensure the maximum possible accuracy. The ADCAL.EXE calibration program leads you through the whole A/D offset and gain adjustment procedure. The basic steps are outlined below:

1. Set analog input channel AI0 as single-ended, bipolar, range ±5 V and connect to the ground.
2. Read TP1 as $V_{G1}$.
3. Change AI0 range to ±0.625 V and read TP1 as $V_{G8}$.
4. Adjust VR4 until -0.05 mV < $V_{G1}$ - $V_{G8}$ < 0.05 mV.
5. Repeat steps 1 ~ 4 until ther is no more need to adjust VR4.
6. Set analog input channel AI0 as single-ended, bipolar, range ±5 V, and set AI1 as single-ended, unipolar, range 0 to 10 V.
7. Connect a DC voltage source with value equal to 0.5 LSB (-4.9959 V) to AI0.
8. Adjust VR2 until the output codes from the card's AI0 flickers between 0 and 1.
9. Connect a DC voltage source with a value of 4094.5 LSB (4.9953 V) to AI0.

10. Adjust VR1 until the output codes from the card's AI0 flickers between 4094 and 4095.
11. Repeat step 7 to step 10, adjusting VR2 and VR1.
12. Connect a DC voltage source with value equal to 2047.5 LSB (4.9959 V) to AI1.
13. Adjust VR3 until the output codes from the card's AI1 flickers between 2047 and 2048.

| A/D code | | Mapping Voltage | |
|---|---|---|---|
| **Hex.** | **Dec.** | **Bipolar ± 5V** | **Unipolar 0 to 10V** |
| 000h | 0 | -4.9971V | 0V |
| 7FFh | 2047 | -0.0024V | 4.9947V |
| 800h | 2048 | 0V | 4.9971V |
| FFFh | 4095 | +4.9947V | 9.9918V |

APPENDIX A

# 82C54 Counter Chip Functions

# A.1 Introduction

The PCI-1713 uses one Intel 82C54 compatible programmable interval timer/counter chip. This popular 82C54 offers three independent 16-bit counters, counter 0, counter 1 and counter 2. Counter 0 is not available for users. Counter 1 is cascaded with counter 2 to create a 32-bit timer for the pacer trigger. A low-to-high edge of counter 2 output can trigger an A/D conversion, and users can utilize this signal as a synchronous signal for other applications.

# A.2 Counter Read/Write and Control Registers

The 82C54 programmable interval timer uses four registers at addresses BASE + 24(Dec), BASE + 26(Dec), BASE + 28(Dec) and BASE + 30(Dec) for read, write and control of counter functions. Register functions appear below:

| Register | Function |
|---|---|
| BASE + 24(Dec) | Counter 0 read/write |
| BASE + 26(Dec) | Counter 1 read/write |
| BASE + 28(Dec) | Counter 2 read/write |
| BASE + 30(Dec) | Counter control word |

Since the 82C54 counter uses a 16-bit structure, each section of read/write data is split into a least significant byte (LSB) and most significant byte (MSB). To avoid errors it is important that you make read/write operations in pairs and keep track of the byte order.

The data format for the control register appears below:

| BASE+30(Dec) | 82C54 control, standard mode | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit** | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Value** | SC1 | SC0 | RW1 | RW0 | M2 | M1 | M0 | BCD |

## Description:

**SC1 & SC0** Select counter.

| Counter | SC1 | SC0 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| Read-back command | 1 | 1 |

**RW1 & RW0** Select read/write operation

| Operation | RW1 | RW0 |
|---|---|---|
| Counter latch | 0 | 0 |
| Read/write LSB | 0 | 1 |
| Read/write MSB | 1 | 0 |
| Read/write LSB first, then MSB | 1 | 1 |

**M2, M1 & M0** Select operating mode

| M2 | M1 | M0 | Mode | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Stop on terminal count |
| 0 | 0 | 1 | 1 | Programmable one shot |
| X | 1 | 0 | 2 | Rate generator |
| X | 1 | 1 | 3 | Square wave rate generator |
| 1 | 0 | 0 | 4 | Software triggered strobe |
| 1 | 0 | 1 | 5 | Hardware triggered strobe |

**BCD** Select binary or BCD counting.

| BCD | Type |
|---|---|
| 0 | Binary counting 16-bits |
| 1 | Binary coded decimal (BCD) counting |

If you set the module for binary counting, the count can be any number from 0 up to 65535. If you set it for BCD (Binary Coded Decimal) counting, the count can be any number from 0 to 9999.

If you set both SC1 and SC0 bits to 1, the counter control register is in read-back command mode. The control register data format then becomes:

| BASE + 30(Dec) 82C54 control, read-back mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit** | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Value** | 1 | 1 | CNT | STA | C2 | C1 | C0 | X |

**CNT = 0** Latch count of selected counter(s).

**STA = 0** Latch status of selected counter(s).

**C2, C1 & C0** Select counter for a read-back operation.

C2 = 1 select Counter 2

C1 = 1 select Counter 1

C0 = 1 select Counter 0

If you set both SC1 and SC0 to 1 and STA to 0, the register selected by C2 to C0 contains a byte which shows the status of the counter. The data format of the counter read/write register then becomes:

| BASE + 24/26/28(Dec) Status read-back mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit** | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **Value** | OUT | NC | RW1 | RW0 | M2 | M1 | M0 | BCD |

**OUT** Current state of counter output

**NC** Null count is 1 when the last count written to the counter register has been loaded into the counting element

# A.3 Counter Operating Modes

## MODE 0 – Stop on Terminal Count

The output will initially be low after you set this mode of operation. After you load the count into the selected count register, the output will remain low and the counter will count. When the counter reaches the terminal count, its output will go high and remain high until you reload it with the mode or a new count value. The counter continues to decrement after it reaches the terminal count. Rewriting a counter register during counting has the following results:

1. Writing to the first byte stops the current counting.
2. Writing to the second byte starts the new count.

## MODE 1 – Programmable One-shot Pulse

The output is initially high. The output will go low on the count following the rising edge of the gate input. It will then go high on the terminal count. If you load a new count value while the output is low, the new value will not affect the duration of the one-shot pulse until the succeeding trigger. You can read the current count at any time without affecting the one-shot pulse. The one-shot is retriggerable, thus the output will remain low for the full count after any rising edge at the gate input.

## MODE 2 – Rate Generator

The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the counter register. If you reload the counter register between output pulses, the present period will not be affected, but the subsequent period will reflect the value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. You can thus use the gate input to synchronize the counter.

With this mode the output will remain high until you load the count register. You can also synchronize the output by software.

## MODE 3 – Square Wave Generator

This mode is similar to Mode 2, except that the output will remain high until one half of the count has been completed (for even numbers), and will go low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the state of the output is changed, the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded ) decrements the count by 1. Subsequent clock pulses decrement the count by 2. After time-out, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by two until time-out, then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

## MODE 4 –Software-Triggered Strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period then go high again.

If you reload the count register during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

## MODE 5 – Hardware-Triggered Strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable.

# A.4 Counter Operations

## Read/Write Operation

Before you write the initial count to each counter, you must first specify the read/write operation type, operating mode and counter type in the control byte and write the control byte to the control register [BASE + 30(Dec)].

Since the control byte register and all three counter read/write registers have separate addresses and each control byte specifies the counter it applies to (by SC1 and SC0), no instructions on the operating sequence are required. Any programming sequence following the 82C54 convention is acceptable.

There are three types of counter operations: Read/load LSB, read / load MSB and read /load LSB followed by MSB. It is important that you make your read/write operations in pairs and keep track of the byte order.

## Counter Read-back Command

The 82C54 counter read-back command lets you check the count value, programmed mode and current states of the OUT pin and Null Count flag of the selected counter(s). You write this command to the control word register. Format is as shown at the beginning of this section.

The read-back command can latch multiple counter output latches. Simply set the CNT bit to 0 and select the desired counter(s). This single command is functionally equivalent to multiple counter latch commands, one for each counter latched.

The read-back command can also latch status information for selected counter(s) by setting STA bit = 0. The status must be latched to be read; the status of a counter is accessed by a read from that counter. The counter status format appears at the beginning of the chapter.

## Counter Latch Operation

Users often want to read the value of a counter without disturbing the count in progress. You do this by latching the count value for the specific counter then reading the value.

The 82C54 supports the counter latch operation in two ways. The first way is to set bits RW1 and RW0 to 0. This latches the count of the selected counter in a 16-bit hold register. The second way is to perform a latch operation under the read-back command. Set bits SC1 and SC0 to 1 and CNT = 0. The second method has the advantage of operating several counters at the same time. A subsequent read operation on the selected counter will retrieve the latched value.

APPENDIX B

# PCLD-881B
# Wiring Terminal Board

# B.1 Introduction

The PCLD-881B Screw-terminal Board provides convenient and reliable signal wiring for the PCI-1713 and PCL-813B, both of which have a 37-pin D-type connector.

Due to its special PCB layout you can install passive components to construct your own signal-conditioning circuits. The user can easily construct a low-pass filter, attenuator or current shunt converter by adding resistors and capacitors on to the board's circuit pads.

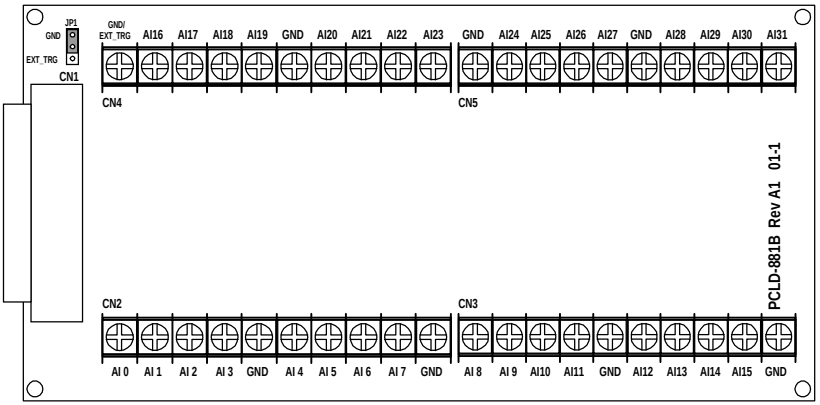
# B.2 Features

- Low-cost screw-terminal board for the PCI-1713 and PCL-813B with 37-pin D-type connector
- 40 terminal points for one 37-pin D-type port
- Reserved space for signal-conditioning circuits such as low-pass filter, voltage attenuator and current shunt
- Industrial type termination blocks permit heavy-duty and reliable signal connections
- Table-top mounting using nylon standoffs. Screws and washers provided for panel or wall mounting
- Dimensions: 218mm (W) x 115mm (L) x 31mm (H) (8.6" x 4.5" x 1.2")

# B.3 Application

- Field wiring for the PCI-1713 and PCL-813B equipped with 37-pin D-type connector.

# B.4 Board Layout


JP1
GND
EXT_TRG
CN1
GND/
EXT_TRG
AI16 AI17 AI18 AI19 GND AI20 AI21 AI22 AI23
GND AI24 AI25 AI26 AI27 GND AI28 AI29 AI30 AI31
CN4
CN5
PCLD-881B Rev A1 01-1
CN2
CN3
AI 0 AI 1 AI 2 AI 3 GND AI 4 AI 5 AI 6 AI 7 GND
AI 8 AI 9 AI10 AI11 GND AI12 AI13 AI14 AI15 GND

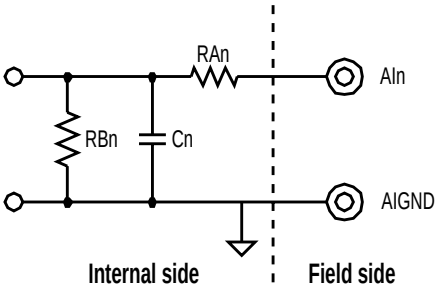
**CN1**: 37-pin D-type connector for connection to the PCI-1713 or PCL-813B

**CN2 ~ 5**: 10-pin wiring terminal block for analog input

**JP1**: Connecting pin 1 of CN4 to the ground (default setting) or to float for an external trigger source.

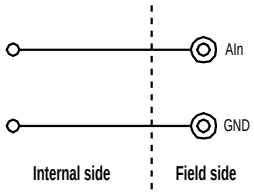
***Note!***: *When configuring for the PCI-1713, the user can either short the upper two pins of JP1 to connect pin 1 of CN4 to ground, or short the lower two pins of JP1 to float pin 1 of CN4 for connection to an external trigger source. However, when configuring for the PCL-813B, the user has to short the upper two pins of JP1 because no external trigger is supported.*

# B.5 Single-ended Connections



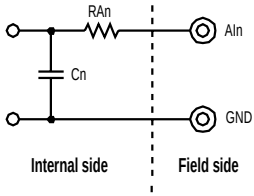

where n = 0, 1, 2, ....., 31

**a)** Straight-through connection (factory setting)
RAn = 0 Ω (short)
RBn = none
Cn = none



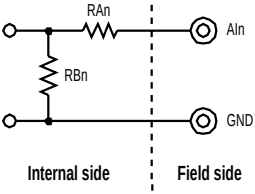

**b)** 1.6 kHz (3dB) low pass filter
RAn = 10 kΩ
RBn = none
Cn = 0.01μF

$$f_{3dB} = \frac{1}{2\pi RAnCn}$$

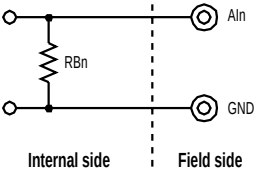



**c)** 10 : 1 voltage attenuator:
RAn = 9 kΩ
RBn = 1 kΩ
Cn = none

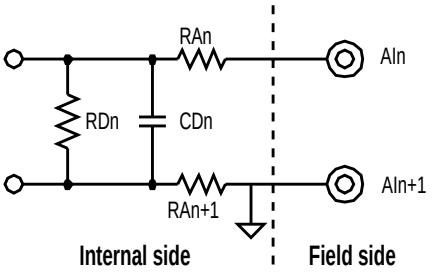
$$\text{Attenuation} = \frac{RBn}{RAn + RBn}$$




**d)** 4 ~ 20 mA to 1 ~ 5 $V_{DC}$ signal converter:
RAn = 0 Ω (short)
RBn = 250 Ω (0.1% precision resistor)
Cn = none

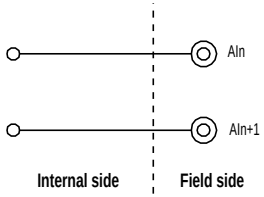


# B.6 Differential Connections



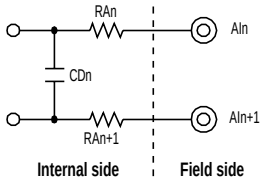

where n = 0, 2, 4, ....., 30

**a)** Straight-through connection (factory setting):
RAn = 0 Ω (short)
RAn+1 = 0 Ω (short)
RDn = none
CDn = none



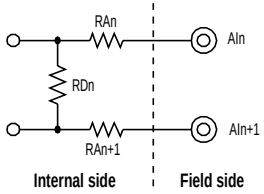

**b)** 1.6 kHz (3dB) low pass filter
RAn = 5 kΩ
RAn+1 = 5 kΩ
RDn = none
CDn = 0.01μF

$$f_{3dB} = \frac{1}{2\pi(RAn + RAn+1)\,CDn}$$

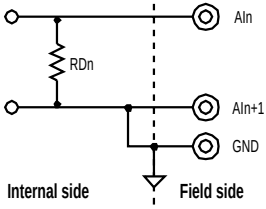



**c)** 10 : 1 voltage attenuator:
RAn = 4.5 kΩ
RAn+1 = 4.5 kΩ
RDn = 1 kΩ
Cn = none

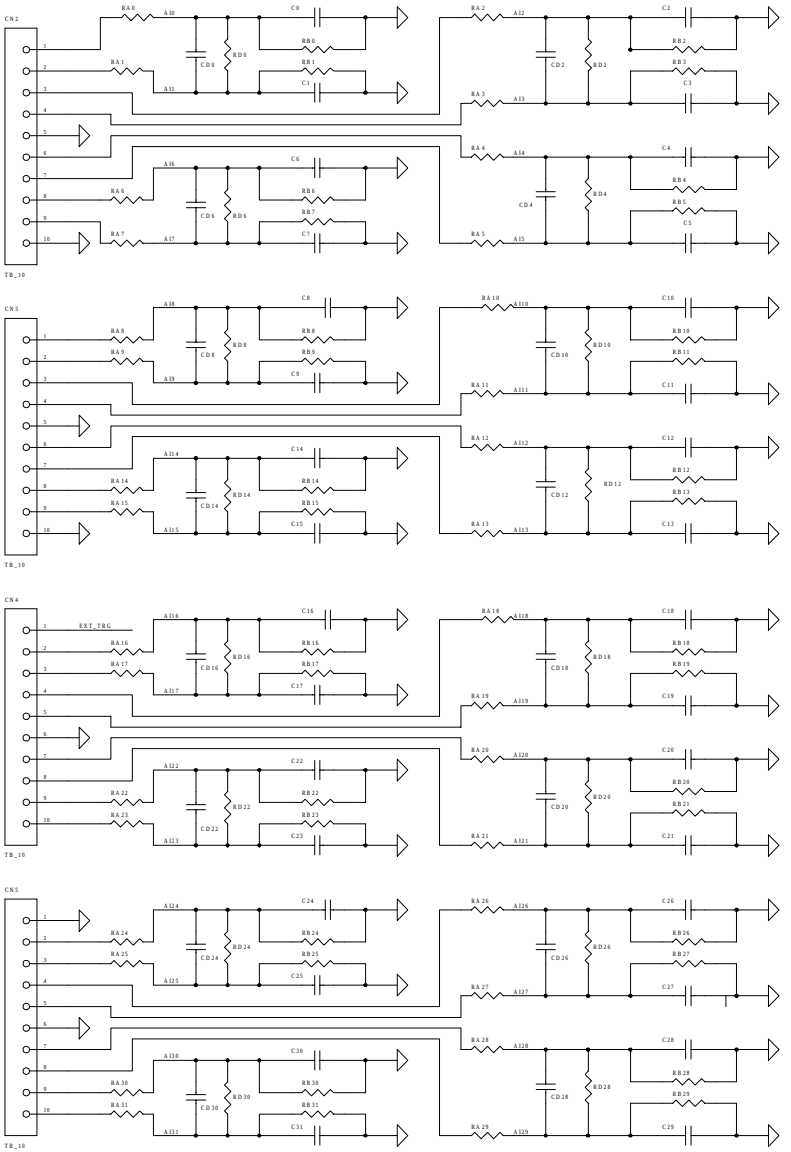
$$\text{Attenuation} = \frac{RDn}{RAn + RAn+1 + RDn}$$

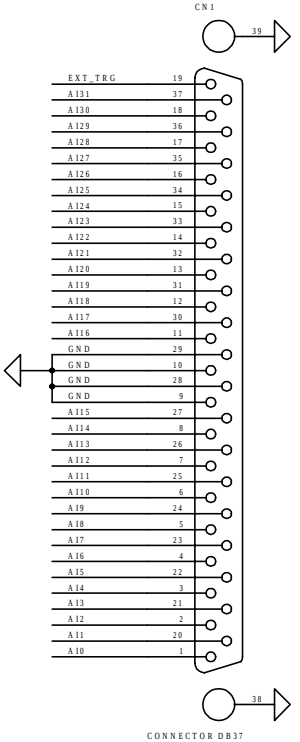


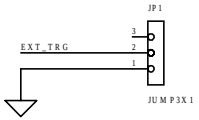

**d)** 4 ~ 20 mA to 1 ~ 5 $V_{DC}$ signal converter:
RAn = 0 Ω (short)
RAn+1 = 0 Ω (short)
RDn = 250 Ω (0.1% precision resistor)
CDn = none



# B.7 Technical Diagram




CN1
39
EXT_TRG 19
AI31 37
AI30 18
AI29 36
AI28 17
AI27 35
AI26 16
AI25 34
AI24 15
AI23 33
AI22 14
AI21 32
AI20 13
AI19 31
AI18 12
AI17 30
AI16 11
GND 29
GND 10
GND 28
GND 9
AI15 27
AI14 8
AI13 26
AI12 7
AI11 25
AI10 6
AI9 24
AI8 5
AI7 23
AI6 4
AI5 22
AI4 3
AI3 21
AI2 2
AI1 20
AI0 1
38
CONNECTOR DB37


JP1
3
2
1
EXT_TRG
JUMP3X1